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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,933	03/16/2004	Akiyoshi Aoyagi	9319S-000670	2339
27572	7590	06/30/2005	EXAMINER	
HARNES, DICKEY & PIERCE, P.L.C.			SANDVIK, BENJAMIN P	
P.O. BOX 828			ART UNIT	
BLOOMFIELD HILLS, MI 48303			PAPER NUMBER	
			2826	

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/801,933

Applicant(s)

AOYAGI, AKIYOSHI

Examiner

Ben P. Sandvik

Art Unit

2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) 2,6,7 and 14-16 is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1,3-5 and 8-13 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: ____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3, 4 are rejected under 35 U.S.C. 102(e) as being anticipated by Degani et al (U.S. PG Pub #20020079568).

With respect to **claim 1**, Degani teaches a first carrier substrate (Fig. 6, 76), a first semiconductor chip mounted face down on the first carrier substrate (Fig. 6, 75), a second semiconductor chip mounted face down on a reverse face of the first carrier substrate (Fig. 6, 74), a second carrier substrate (Fig. 6, 81), a third semiconductor chip mounted on the second carrier substrate (Fig. 6, 77), and protruding electrodes connecting the second carrier substrate to the first carrier substrate so that the second carrier substrate is held above the first semiconductor chip (Fig. 7, 92).

With respect to **claim 3**, Degani teaches a sealant for sealing the third semiconductor chip (Fig. 3, 38).

With respect to **claim 4**, Degani teaches a sealant that comprises a molded resin (Paragraph 28).

With respect to **claim 5**, Degani teaches a position of a sidewall of the sealant coincides with a sidewall of the second carrier substrate (Fig. 3, 38).

With respect to **claim 8**, Degani teaches a first carrier substrate on which the first semiconductor chip and the second semiconductor chip are mounted further comprises a flip-chip mounted ball grid array (Fig. 6, Paragraph 36), and wherein the second carrier substrate on which the third semiconductor chip is mounted further comprises at least one of a mold-sealed ball grid array and a chip size package (Fig. 6, Paragraph 36).

With respect to **claim 10**, Degani teaches a device wherein the third semiconductor chip comprises a structure in which a plurality of chip is arranged in parallel on the second carrier substrate (Fig. 6, 77, 78, 79).

With respect to **claim 11**, Degani teaches a first carrier substrate (Fig. 6, 81), a first semiconductor chip mounted face down on at least one face of the first carrier substrate (Fig. 6, 77), a second carrier substrate (Fig. 6, 76), a second semiconductor chip mounted on the second carrier substrate (Fig. 6, 75), a third semiconductor chip mounted on a reverse face of the second carrier substrate (Fig. 6, 74), and protruding electrodes bonding the second carrier substrate to the first carrier substrate (Fig. 7, 92).

With respect to **claim 12**, Degani teaches a carrier substrate (Fig. 6, 76), a first semiconductor chip mounted face down on the carrier substrate (Fig. 6, 75), a second semiconductor chip mounted face down on a reverse face of the carrier substrate (Fig. 6, 74), a third semiconductor chip on which re-arrangement wiring

Art Unit: 2826

line layers are formed on surfaces where electrode pads are formed (Fig. 7, 91, 93, 94), and protruding electrodes connecting the third semiconductor chip to the carrier substrate so that the third semiconductor chip is held above the first semiconductor chip (Fig. 7, 92).

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 13 is rejected under 35 U.S.C. 102(b) as being anticipated by Akram et al (U.S. PG Pub #20010015488).

With respect to **claim 13**, a first carrier substrate (Fig. 1, 140), a first electronic part mounted on the first carrier substrate (Fig. 1, 150), a second electronic part mounted on a reverse face of the first carrier substrate (Fig. 1, 162), a second carrier substrate (Fig. 1, 116), a third electronic part mounted on the second carrier substrate (Fig. 1, 128), protruding electrodes connecting the second carrier substrate to the first carrier substrate so that the second carrier substrate is held above the first electronic part (Fig. 1, 148), and a sealant for sealing the third electronic part (Fig. 1, 170).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben P. Sandvik whose telephone number is (571) 272-8446. The examiner can normally be reached on Mon-Fri.

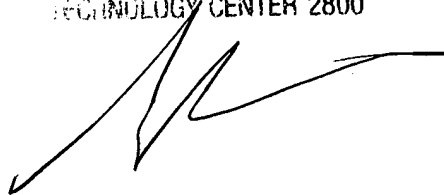
Art Unit: 2826

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

bps

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

A handwritten signature in black ink, appearing to be 'Nathan J. Flynn', written over the printed name and title.